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#4 Election

6/18/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

HASHIMOTO, Hiroshi et al.

Group Art Unit: **2813**

Serial No.: **09/960,399**

Examiner: **Chandra CHAUDHARI**

Filed: **September 24, 2001**

P.T.O. Confirmation No.: **5652**

For: **SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS THEREOF**

RESPONSE TO THE RESTRICTION REQUIREMENT DATED May 13, 2002

Commissioner for Patents
Washington, D.C. 20231

Date: June 11, 2002

Sir:

This paper is submitted in response to the Official Action dated **May 13, 2002**.

In the Action, restriction is required between Group (I), Claims 1-15, drawn to a method of making a semiconductor device; and Group (II), Claims 16-18, drawn to a semiconductor device.

Applicants hereby elect the subject matter of Group (II), Claims 16-18 prosecution in this application. This election is made without traverse, it being understood that the applicants' rights to the filing of a divisional application directed to the non-elected subject matter under 35 USC 120 and 35 USC 121 are retained.

In the event that this paper is not timely filed, applicants hereby petition for an appropriate extension of time. The fee for any such extension may be charged to our Deposit Account No. 01-2340.

In the event any additional fees are required in connection with this response, please charge our Deposit Account No. 01-2340.

Respectfully Submitted,

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